

# Synopsys Timing Constraints And Optimization

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The Galaxy Constraint Analyzer is an intuitive tool that enables designers to quickly assess the correctness and consistency of timing constraints. Correctness and consistency lead to more efficient runtimes in Synopsys' Design Compiler® synthesis and IC Compiler physical implementation tools.

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constraints: rules from library vendor for proper functioning of the fabricated circuit Must not be violated Common constraints: transition time, fanout load, capacitance Design optimization . constraints: user-specified timing and area optimization goals DC tries to optimize these without violating design rules Common constraints: timing and area

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